AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

At page 3, lines 19-27, and page 4, lines 1-2:

In the present invention, in order to achieve the above-described objects, primitive cells, which are circuit patterns corresponding to each of the constituent elements of the semiconductor device, are arranged in the element formation area of the semiconductor device, and at least one fill cell with a diffusion layer and no wiring is arranged in a vacant area that is generated in the element formation area after all primitive cells have been arranged. Since the fill cells are arranged so as to make the data ratio of the diffusion layer (area ratio of the diffusion layer) falls within a prescribed range, uneven distribution of the diffusion layers is eliminated, whereby a wafer having a uniform surface can be obtained even when CMP is conducted to remove the insulating film on a wafer having diffusion layers and trenches formed thereon.

At page 4, lines 24-26:

The above and ~~add~~ other objects, features, and advantages of the present invention will become apparent from the following description with reference to the accompanying drawings, which illustrate examples of the present invention.

At page 6, lines 18-25:

In accordance with instructions from an operator that are supplied as input by way of input device 2, each of the constituent elements whose data are stored in netlist storage

unit 4 are grouped in advance. Each group contains constituent elements having related operations, such as constituent elements sending and/or receiving a signal to each other, and constituent elements that are necessary for realizing specific functions. At this time, data of each constituent element are stored in netlist storage unit 4 in correspondence with group information that indicates the group to which the constituent element belongs.

At page 9, lines 2-11:

Integrator 1-3 integrates the circuit patterns of each layer of the semiconductor device formed by unit for arrangement and wiring 1-2 to complete the layout pattern in the element formation area. The layout pattern data produced by integrator 1-3 may be in a layout format showing the actual ~~actually~~ arrangement of each constituent element, and also may be in a format of combination of identifiers for identifying primitive cells and fill cells. Although the layout format simplifies the processing of subsequent steps, this layout format results in an increase in the amount of layout pattern data. On the other hand, the format of combination of identifiers reduces the amount of layout pattern data, but results in more complex processing in subsequent steps.